IN THE CLAIMS

Claim 1 (Canceled).

Claim 2 (Previously Presented): An array substrate for a flat-panel display comprising:

a plurality of scanning lines;

a plurality of signal lines arranged substantially perpendicular to the scanning lines through a first insulator film therebetween;

switching elements respectively disposed in a vicinity of each intersection of the scanning and signal lines, a terminal of each switching element being electrically connected with a signal line;

a second insulator film covering such multi layer wiring pattern;

pixel electrodes arranged in a matrix as to respectively correspond to said each intersection, on the second insulator film;

pixel-electrode contact holes perforating the second insulator film as to electrically connect another terminal of each switching element to a pixel electrode;

an area containing wire breakage to a signal or scanning line;

a pair of contact holes perforating the second insulator film as to expose an upper face of said signal or scanning line, at wire portions interlaying the area containing wire breakage;

a bypass wire extending from one to another of the pair of contact holes to detour a vicinity of the area containing wire breakage and to electrically connect said wire portions interlaying the area containing wire breakage;

a pixel-electrode cutout being formed by rectangularly removing a pixel electrode throughout an area ranging from the vicinity of the area containing wire breakage to a place receiving the bypass wire, which extends along an edge of the pixel-electrode cutout.

Claim 3 (Previously Presented): An array substrate according to claim 2,

further comprising a light-insulator film arranged to entirely cover an area that is within the pixel-electrode cutout and is surrounded by the area containing wire breakage, the bypass wire and said wire portions interlaying the area containing wire breakage.

Claim 4 (Original): An array substrate according to claim 2 or 3,

said bypass wire being spaced apart from the pixel electrode as to prevent electrical contact between them.

Claim 5 (Canceled).

Claim 6 (Canceled).

Claim 7 (Previously Presented): A method for manufacturing an array substrate for a flat-panel display comprising a plurality of scanning lines; signal lines arranged substantially perpendicular to the scanning lines; pixel electrodes arranged in a matrix, each corresponding with respective of intersections of the scanning lines and the signal lines; and switching elements, each being disposed in a vicinity of respective of said intersections as to input signal from the signal line to the pixel electrode; comprising:

forming a series of film formations and patterning for achieving an arrangement of the signal lines and the scanning lines and the switching elements described for the flat-panel display;

detecting a wire breakage on a wire within a pixel area and detecting a position of the wire breakage;

forming a cutout, which is a solid region cut out from a linear fringe on one of the pixel electrodes by removing a conductive film comprising said one of the pixel electrodes at a vicinity of the wire breakage, on one or both areas demarcated by said wire having the wire breakage, by laser irradiation; and

forming a bypass wire detouring the wire breakage and electrically connecting two wire parts interlaying the wire breakage, by sequential or continuous depositing of a conductive layer at an inside edge of said cutout to run along the edge of said cutout at a preset distance from said edge, using laser CVD technique.

Claim 8 (Previously Presented): A method for manufacturing an array substrate for a flat-panel display comprising:

a series of film formations and patterning for forming a plurality of scanning lines; signal lines arranged substantially perpendicular to the scanning lines with a first insulator film therebetween; and switching elements each being disposed in vicinity of respective one of intersections of the scanning lines and the signal lines and having a terminal electrically connected with the signal line; and thereby forming a multi-layer wire pattern including the scanning and signal lines and the switching elements;

forming a second insulator film covering the multi-layer wire pattern;

forming pixel electrodes being arranged in a matrix each to correspond with respective one of said intersections, on the second insulator film;

forming pixel-electrode contact holes for perforating the second insulator film as to connect another terminal of the switching element to the pixel electrode; further comprising:

detecting a wire breakage on a wire within a pixel area and position of the wire breakage;

forming a cutout, which is a solid region cut out from a linear fringe on one of the pixel electrodes by removing a conductive film comprising said one of the pixel electrodes at vicinity of the wire breakage, on one or both of areas demarcated by said wire having the wire breakage, by wire breakage; and

forming a bypass wire detouring the wire breakage and electrically connecting two wire parts interlaying the wire breakage, by sequential or continuous depositing of a conductive layer at inside of edge of said cutout to run along the edge of said cutout with a preset distance from said edge, using laser CVD technique.

Claim 9 (Previously Presented): A method for manufacturing an array substrate according to the claim 7 or 8, further comprising:

depositing a conductive layer by laser CVD technique to an area that is within said cutout and is surrounded by the bypass wire, the wire breakage and wire portions interlaying the wire breakage, as to form a pattern of a light insulator film entirely covering said area, after the forming of the bypass wire.

Claims 10-12 (Canceled).

Claim 13 (Previously Presented): A method for manufacturing an array substrate according to the claim 7 or 8, wherein

when the wire breakage is determined to be due to interposing of a foreign matter, then said forming of the cutout and said forming of the bypass wire is made, and

when the wire breakage is determined to be due to other cause, then a connecting wire extending along said wire is formed by CVD technique.

Claims 14-17 (Canceled).

Claim 18 (Previously Presented): An array substrate according to claim 3, wherein the light-insulator film overlaps inner fringe of the bypass wire.

Claim 19 (Previously Presented): An array substrate according to claim 18, wherein the light-insulator film directly overlaps the inner fringe of the bypass wire.

Claim 20 (Previously Presented): An array substrate according to claim 3, wherein the light-insulator film is integrally formed with the bypass wire.

Claim 21 (Previously Presented): A method for manufacturing an array substrate according to the claim 9, wherein the light-insulator film overlaps inner fringe of the bypass wire.

Claim 22 (Previously Presented): A method for manufacturing an array substrate according to the claim 9, wherein the light-insulator film is formed simultaneously with the bypass wire.

Claim 23 (Previously Presented): A method for manufacturing an array substrate according to the claim 7 or 8, wherein said cutout is a solid rectangular region.